Electrical Performance of Bumpless Build-Up Layer Packaging

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Abstract

The Bumpless Build-Up Layer (BBUL) microelectronic packaging technology is characterized by the absence of a conventional substrate core and a direct extension of the outmost metallization layers of the die into the overall thin substrate. Such a coreless, thin package provides the advantages of small electrical loop inductance for power delivery and minimized discontinuities for high-speed signaling. Furthermore, it allows for reduced thermomechanical stresses on low dielectric constant (low-*k*) die materials, high lead count, and ready integration of multiple electronic, optical, and microelectromechanical components. BBUL is also expected to be compatible with innovative thermal solutions using frontside heat removal.

After summarizing some of the non-electrical characteristics of the BBUL packaging technology we conduct transient electromagnetic (EM) simulations for the core power delivery problem. A simplistic lumped-element theory, valid for the first few nanoseconds of the transient core switching noise waveforms, is laid out initially. We then obtain distributed die voltage time-domain results for a standard six-layer flip-chip package and compare them with a model of a similar, but much thinner, three-layer BBUL package. Finally, a package capacitance reduction study indicates that a thin package as implemented by the BBUL technology and presenting a substantially reduced package loop inductance calls for the introduction of an intermediate level of decoupling in between the conventional on-die high-frequency decoupling and the on-package mid-frequency decoupling stages.

Introduction

Future generations of microprocessors are expected to have larger numbers of signal leads, stricter control of impedance and crosstalk on these lines, and greater demands for power delivery and heat extraction. For microelectronic packaging, major challenges are electrical performance in terms of power and signal integrity, thermal management, and thermomechanical reliability, especially in view of the advent of low dielectric constant (low-k) on-die materials. Continued reduction in end product size requires a package with a small form factor that allows for dense placement of input and output electrical connections. Future microprocessors may also require integration of multiple chips or other electrical and optical components on the same package. This accumulation of demands stretches or exceeds the capabilities of current packaging technologies, such as flip-chip pin grid array (FCPGA) packaging [1].

Some of the issues mentioned above could be addressed with a chip-scale package (CSP) in which the package redistribution layers are built up on top of the die [2]–[5]. However, packaging advanced logic chips makes additional demands that require the area of the package to be considerably larger than the area of the chip.

The bumpless build-up layer (BBUL) packaging technology [6] is designed to meet requirements for 65 nm generation silicon technology and beyond.

After summarizing briefly some of the non-electrical characteristics of BBUL, in the present paper we concentrate on the power delivery benefits enabled by BBUL, as compared to the electrical performance of a standard FCPGA package.

Non-electrical attributes of BBUL

BBUL differs from traditional packages in that it embeds dice in a co-planar substrate, which has build-up layers formed on top of it. A standard microvia formation process, such as laser drilling, makes the connections between the build-up layers and the die bond pads. This is analogous to a wafer level CSP (WLCSP), but with the die embedded in the panel to increase area. The build-up layers are made with a standard high-density integration (HDI) patterning technology.

The BBUL structure offers routing advantages compared to flip-chip interconnection, contributing to a potentially reduced package layer count. Via size and alignment capabilities of HDI via formation processes allow a tighter pitch for the die-package interconnections compared to flip-chip. Unlike many versions of flip-chip assembly, die-package interconnections can be arbitrarily placed, because no restriction is imposed by limitations of the flip-chip underfill process. This capability provides a significant advantage in the number of signals that can be routed out from the die on a single layer.

BBUL technology allows the overall package to be very thin. The thickness of the package will exceed the die thickness by 100 μm or less, depending on the thermal and socketing solution used. This attribute is attractive for mobile applications and also a main contributing factor to the improvements offered by BBUL in terms of power delivery and mechanical stress.

Incorporation of fragile, low dielectric constant (low-k) materials into the back end interconnect structures of silicon devices requires minimization of stresses induced on these structures. BBUL has been shown numerically to impose reduced stresses when compared to the model of an organic flip-chip package with bumps of high lead content [7].

Thermal issues are critical for future microprocessor products and few cost effective solutions are known. When combined with standard heat removal schemes BBUL performs similarly to conventional flip-chip packaging [6]. However, it is plausible that the thinness of BBUL will support the introduction of tailored thermal solutions that take advantage of its unique structure. In particular, frontside heat removal through the coreless substrate of BBUL is a promising option that may lead to significant thermal improvements.

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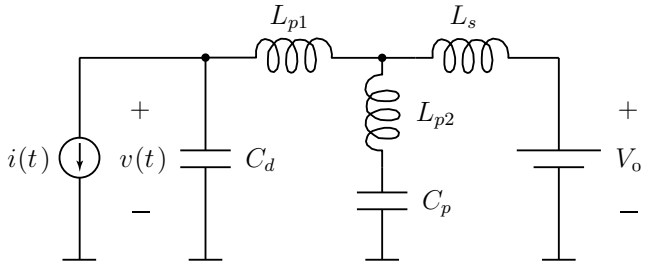

Figure 1: Lumped-element model of a power delivery structure.

Lumped-element power delivery modeling

Figure 1 shows a simplified, non-resistive lumped-element model of a power delivery structure involving an active die, a package, and a DC voltage supply [8]. For a quiet die we have $i(t) = I_0 = \text{const.}$ with I_0 a leakage current flowing through the package inductance L_{p1} and the inductance L_s in between the package and the power supply located somewhere else, e.g., on a motherboard. The supply voltage V_0 appears as $v(t)$ across the on-die, high-frequency decoupling capacitance C_d that is inactive in the DC case, similar to the on-package, mid-frequency decoupling capacitance C_p with its associated parasitic inductance L_{p2}.

Typical dice are capable of generating large average current swings between low and full power states, due to their large number of transistors and high internal clock speeds. Simply speaking, typical transitions will draw a large current from the package which, in a simplistic manner, can be modeled as an independent current source described as

$$i(t) = I_0 + \Delta I\, u(t) \tag{1}$$

where ΔI is the current step and $u(t)$ the unit step function. During the first few nanoseconds following the current step the relative large inductance L_s effectively isolates the power supply from the rest of the circuit and, letting $L_s \to \infty$, the inductances L_{p1} and L_{p2} in Fig. 1 combine as

$$L_p = L_{p1} + L_{p2} \tag{2}$$

where L_p is referred to in the following as the loop inductance of the package. The initial-value problem is readily solved using a frequency domain formalism. Denoting the Laplace transform of the transient portion of $v(t)$ as $\tilde{V}(s)$ with the complex frequency s we have

$$\tilde{V}(s) = -\frac{\Delta I}{s}\left[s\,C_d + \frac{1}{s\,L_p + 1/\left(s\,C_p\right)}\right]^{-1} \tag{3}$$

Rewriting (3) we find

$$\tilde{V}(s) = -\frac{\Delta I}{C_d + C_p}\left[\frac{C_p/C_d}{s^2 + \left(C_d + C_p\right)/\left(L_p\,C_d\,C_p\right)} + \frac{1}{s^2}\right] \tag{4}$$

which readily leads to

$$\begin{aligned} v(t) \quad = \quad & V_0 - \frac{\Delta I\, u(t)}{1 + C_d/C_p}\left[\frac{1}{C_d}\sqrt{\frac{L_p}{1/C_d + 1/C_p}}\right. \\ & \left. \times \sin\left(\sqrt{\frac{1/C_d + 1/C_p}{L_p}}\,t\right) + \frac{t}{C_p}\right] \end{aligned} \tag{5}$$

Equation (5) describes the combination of oscillations of the resonator formed by decoupling capacitance and loop inductance on one hand, and the progressing discharging of the capacitors on the other.

Initially, all the charge is drawn from the on-die capacitance C_d. Note how this picture formally follows from (5) by considering

$$v(t) \sim V_0 - \Delta I\,\frac{t}{C_d} \quad \text{as} \quad t \to 0^+ \tag{6}$$

Similarly, at late times when

$$t \gg \frac{C_p}{C_d}\sqrt{\frac{L_p}{1/C_d + 1/C_p}} \tag{7}$$

we have, as expected,

$$v(t) \sim V_0 - \Delta I\,\frac{t}{C_d + C_p} \tag{8}$$

For typical microchips C_p is much larger than C_d. As $C_p \to \infty$, we find that (5) simplifies to [9]

$$v(t) = V_0 - \Delta I\, u(t)\sqrt{\frac{L_p}{C_d}}\,\sin\omega_0 t \tag{9}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_p\,C_d}} \tag{10}$$

The "drooping" of the die voltage as described by (5) and in simplified form by (9) can limit the performance of a microchip. Notice how (9) predicts a first voltage minimum at time

$$t_1 = \frac{\pi}{2}\sqrt{L_p\,C_d} \tag{11}$$

The magnitude of this "first droop" is given by

$$V_1 = \Delta I\sqrt{\frac{L_p}{C_d}} \tag{12}$$

Thus, drooping of voltages on power planes below their minimum allowed values may occur if decoupling is not adequate. Care must be taken in the package design to ensure that the voltage provided to the die remains within often stringent specifications. Failure to do so can result in timing violations or reduced component lifetime.

Equation (5) and (9) display a square root dependence of voltage drooping on loop inductance explicitly. BBUL targets the reduction of the inductance L_{p1} in Fig. 1 and (2) by reducing the thickness of the package and elimination of plated through-holes (PTHs). This in turn may allow usage of a smaller on-package capacitance C_p with lower associated parasitic inductance L_{p2}. Thus, the loop inductance L_p of the package can be reduced significantly. In the following section we demonstrate this by simulations based on an actual package design, quantifying the improvement in loop inductance BBUL is expected to provide.

Please note that the validity of the simple lumped-element power delivery analysis described above is restricted to the early portion of the response, as indicated by the unbounded behavior of (5). A correct description at later times needs to take into account losses and, more importantly, the influence of the power distribution system beyond the boundaries of the package [10].

Transient design-based power delivery simulations

We obtain power delivery time-domain results for a standard six-layer flip-chip package and compare them with a model of a similar three-layer BBUL package.

Power delivery simulation methodology

The simulations are carried out using a signal and power integrity tool [11] that incorporates EM wave propagation through the multiple layers of the often complex package structures. The underlying numerical algorithm couples multiple instances of circuit, multiconductor transmission line (MTL), and two-dimensional (2-D) finite-difference time domain (FDTD) solvers. The interactions between different components are introduced through simplified models of the local physics at interfaces that result from the package geometry and electrical design. In particular, the 2-D FDTD computational domains representing power and ground planes of different shapes can be stacked vertically and interconnected by an arbitrary number of vias, yielding a "two-and-a-half-dimensional" (2.5-D) package model of high granularity and exhibiting a tractable computational complexity as compared to a comprehensive three-dimensional (3-D) modeling approach that is not practical today.

Design-based 2.5-D modeling promises the elimination of the process of extracting "parasitics," which is necessary for the, at times, tedious construction of distributed lumped-element circuit models [10] that are characterized by a necessarily relatively low granularity but offer the advantage of the possibility of low computational complexity. Furthermore, once a 2.5-D power delivery model is available, possibly integrating separate power nets that may be coupled through shared ground planes [12], it is possible to study signal integrity for selected input/output (I/O) lines in the presence of the same structures that are used in the power delivery simulations. In the low-frequency or DC limit, high granularity of a power delivery package model is attractive for the identification of local current crowding and package self-heating effects. However, experience has shown that it is generally difficult to design EM algorithms that are valid at both low and high frequencies, especially when physics-based approximations are involved [13]. Finally, it must be pointed out that advanced power delivery structures often are inherently 3-D in certain sub-regions. For example, designers sometimes split power and ground planes in many narrow strips of alternating polarity (power bussing) and such structures are not well described using either metal patches or transmission line systems, although topologically this may be no problem. Other elements in microelectronic power delivery that stretch the 2.5-D concept are PTHs with diameters that can be several times the grid size of the FDTD mesh, leading to an overestimation of package inductance. These cases require the implementation of careful workarounds that may require calibration with the same extraction tools that are used for the construction of distributed models based on lumped circuit elements. Thus a major advantage of the 2.5-D modeling approach (the avoidance of lumped parameter extraction) is diminished.

In any event, the overall methodology employed below should allow a realistic comparison of the electrical performance of BBUL against a standard package for a major microprocessor product. Only the circuit and FDTD solvers of the simulation tool are invoked; there are no transmission lines in the power delivery models considered.

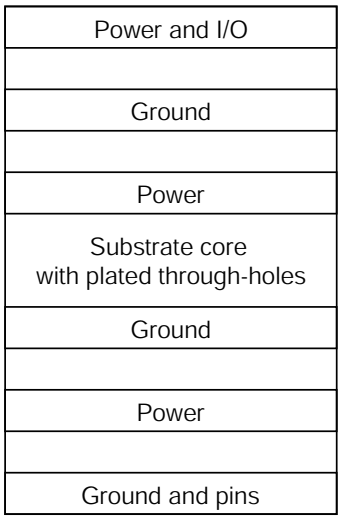

Figure 2: Stack-up of a standard package with six layers and a substrate core.

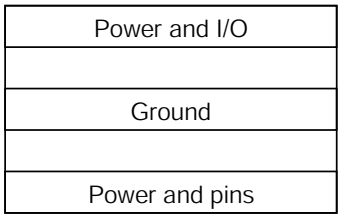

Figure 3: Stack-up of a BBUL package with three layers. Note the absence of a substrate core, making the BBUL package electrically thin.

BBUL versus standard package

The schematic stack-up structures of the two packages are shown in Fig. 2 and 3, respectively, indicating the basic functionality of the different layers.

The power and ground nets of the standard package were extracted from an existing full package design file and translated into the format of the EM simulator, with a resolution of the FDTD meshes of 240×240 grid cells each. Careful manual and semi-automatic editing was then applied to generate a structure that can be simulated successfully. In particular, power bussing structures were replaced by solid power and ground planes. PTHs were modeled as vias with a reduced length and increased resistivity, such that the vias in the simulation exhibit the same inductance and resistance as PTHs simulated separately in a 3-D quasistationary tool. Design details that are meaningless in the context of the EM simulation were removed and clusters of microvias replaced by single vias of equivalent cumulative cross-section; steps such as these help reducing the complexity of the models. The resulting model contains power and ground planes of various shapes and more than 4200 vias; the individual locations of these vias are fully

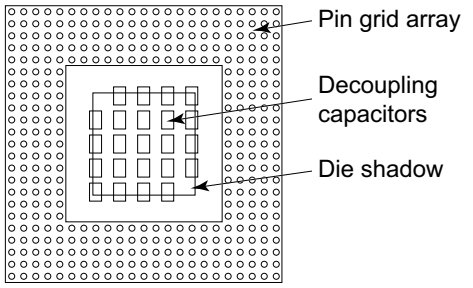

Figure 4: Illustration of discrete decoupling capacitors populating the bottom of a microprocessor package with pin grid array.

taken into account during the simulation. The BBUL package model was generated from the simplified model of the standard package by retaining the top two layers and the bottom layer of the standard package, reversing the polarity of the bottom layer (Fig. 2 and 3), and reconnecting the vias as appropriate. In the resulting BBUL package model based on a realistic design we encounter about 2300 vias.

A distributed 5×5 die model similar to what is shown in [10] and incorporating a power map corresponding to a non-uniformly distributed current load is connected at the top of the packages. In the 2.5-D modeling approach, single microvia pairs used for injecting the load current into the center of each of the 25 package cells can lead to an artificial increase of the package inductance. In other words, the actual die/substrate interface of low inductance in the order of femtohenries formed by a large number of controlled-collapse chip connection (C4) bumps (in the case of the standard flip-chip package) or microvias (in the case of BBUL) is represented incorrectly. We found that an undesired inductance at a connection point in the model can be avoided by creating pairs consisting of two spatially coinciding vias belonging to the power and ground net, respectively. The resistance of the vias can be made arbitrarily small as well.

Land-side decoupling capacitors amounting to a nominal capacitance of $C_p = 23\,\mu\text{F} \gg C_d$ are placed at the bottom of each package (Fig. 4). The lumped parasitic inductance of these capacitors is given by L_{p2} =1.3 pH. As indicated schematically in Fig. 4, generally not the entire die shadow is available for core power decoupling capacitor placement due to the need of an isolated power decoupling solution for sensitive core and system bus phase-locked loops (PLLs) internal to the processor. Another reason for a partial decoupling capacitor depopulation is of course cost to be traded off against power delivery performance.

Finally, in order to concentrate on the vertical current paths underneath the die and different from what was presented in [6], no power supply is connected to the package; there is no socket or motherboard in the simulated models and the pins are left electrically open. Regarding the transient die voltages this configuration corresponds to $L_s \to \infty$ and $V_0 = 0$ in Fig. 1, (5), and (9).

Figure 5 shows the die voltage as obtained from the time-domain EM simulation for the two packages, using identical die, decoupling capacitor, and power supply partial circuits.

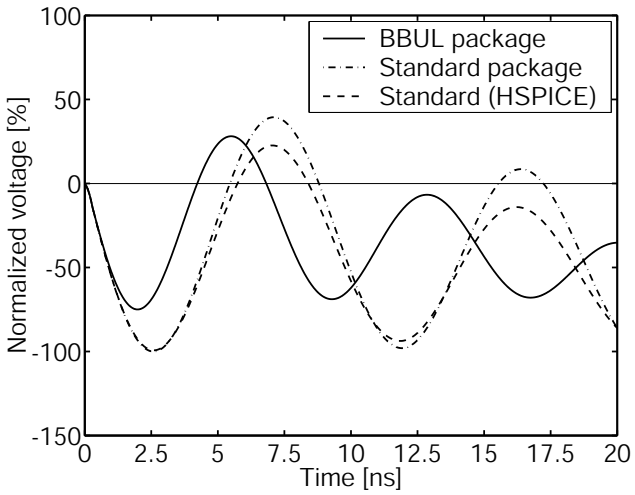

Figure 5: Transient simulation results for the mean die voltage of the two packages, together with HSPICE validation data.

Results from a distributed HSPICE model based on extracted parasitics and representing the standard package are given for comparison. In each case, the voltages across the 25 independent current sources were averaged at each point in time. Notice how the curves in Fig. 5 indeed exhibit a behavior similar to that predicted by (5), up to some damping, the effect of which should be negligible for the first few nanoseconds, in particular at the time the first droop occurs. We point out that the natural frequencies of the resonant switching noise waveforms are observed to be well below 200 MHz, even in the case of the "faster" BBUL package and that the corresponding wavelengths are much larger than the lateral package dimensions. Thus, a lumped-element representation of the package can be adequate, although the quantitative parameterization of the model remains difficult.

But more importantly, the results in Fig. 5 show the significant improvement of the power delivery performance that BBUL can provide. Based on the values of the first droop and using (12), we can quantify this improvement in terms of a few simple numbers.

The magnitude of the first droop is found to be reduced by 25%. Whereas the effective loop inductance L_p of the standard package based on the simulations carried out is calculated to be 3.3 pH, the BBUL package exhibits an L_p of 1.3 pH; this is a reduction by 61%. Evidently, the loop inductance of the BBUL package is dominated by the lumped parasitic inductance L_{p2} of the discrete decoupling capacitors. In terms of the package inductance L_{p1} we have a reduction from 2 pH to 0.03 pH, or by 98.5%. This reduction by almost two orders of magnitude is even more pronounced than one would expect from the mere reduction of the overall thickness of the package substrate by 90%, highlighting the importance of taking into account the details of the package design. One could argue that the elimination of the substrate core, as achieved by the BBUL concept, contributes over-proportionally to the improvement in package inductance due to the large pitch of the core PTHs and the associated large inductance per unit thickness.

The results described above show a clear benefit of BBUL and thin packages in general for power delivery. Further improvements could apparently be made, for example by a dedicated BBUL package design that takes full advantage of the absence of the PTHs. Please note that in the standard package microvias need to land on PTHs and thus the coarse PTH pitch is forced onto parts of the build-up layer design. As a consequence, the BBUL model derived from the standard package design as described above still contains residues of the original PTH configuration, in form of a coarse pitch of some of the microvias.

However, the largest further relative improvement in loop inductance can be achieved by reducing the equivalent series inductance (ESL) of the decoupling capacitors, since for a thin package such as BBUL we have $L_p \approx L_{p2}$, as shown above. Whereas for the standard package a small absolute reduction of L_{p2} leads to only small relative improvement of L_p, in BBUL such reduction by use of lower inductance capacitors translates directly into a power delivery benefit, which may justify selection and further development of such capacitors.

Decoupling capacitors reduction study

Packaging cost is to some extent related to the on-package decoupling solution. We show here that BBUL can offer savings in this respect over standard packaging technology, assuming that both packages were to be designed for the same power delivery performance.

Figure 6 summarizes the results of 2.5-D first droop simulations for two series of packages, representing BBUL and standard packaging, respectively. Within each series the simulated packages are identical up to the number of discrete decoupling capacitors placed on the land-side of the package (Fig. 4). Note that the case $C_p = 23\,\mu$F corresponds to the results in Fig. 5. As C_p is reduced by removing capacitors, parallel decoupling loops disappear and the lumped L_p in (12) increases; thus, the general trend observed in Fig. 6 is expected to behave similar to $1/\sqrt{C_p}$.

We find that the same first voltage droop level (based on averaged die voltages) for a capacitance of 23 μF in the case of the standard package can be achieved with only half the amount of on-package decoupling capacitance when employing BBUL technology. However, oscillations in the next level of the decoupling hierarchy determine a second droop, the magnitude of which depends on the amount of on-package capacitance, similar to the dependence of V_1 on C_d as indicated by (12). Thus, in order to meet a second droop requirement it may be necessary to keep the lumped C_p constant; however, for second droop purposes it matters little how the C_p is distributed on the package. Thus, part of C_p (50% in the numerical example) can be removed from underneath the die and be generated as "bulk" capacitors with relatively large ESL elsewhere on the package. Clearly, BBUL then allows for a reduced on-package capacitor count with associated cost savings.

At the end of the previous section we concluded that first-droop decoupling capacitors for BBUL should have a reduced ESL whereas in the present section we arrived at a more optimal configuration by re-distributing the given on-package capacitance. This suggests that thin packages in general call for the introduction of a new high-to-mid-frequency level in the power decoupling hierarchy, in between the on-die high-frequency decoupling and the on-package mid-frequency decoupling stages.

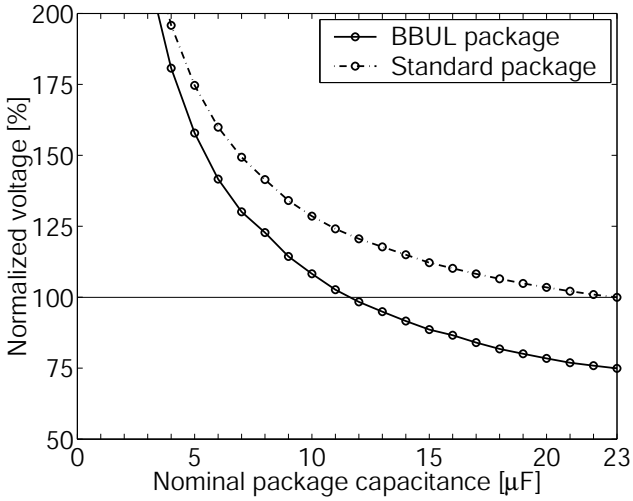

Figure 6: First voltage droop as simulated for packages with varying total decoupling capacitance.

Conclusions

The BBUL microelectronic packaging technology is an attractive alternative to standard flip-chip packaging and constitutes a viable implementation of thin, low-inductance packaging. Based on realistic, design-based simulation models the present paper demonstrates the power delivery advantages of thin packaging from a time domain perspective. The superior electrical performance of BBUL can enable future requirements that cannot be met using standard packaging techniques or lead to concrete cost savings through optimized package designs as shown with help of the example of an on-package capacitors reduction study.

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